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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

re application of:

JOSEPH T. EVANS, JR. ET AL.

Serial No.: 582,672

Filed: September 14, 1990

Group/Class: 233

Examiner: Alyssa H. Bowler

For: NON-VOLATILE MEMORY CIRCUIT USING  
FERROELECTRIC CAPACITOR STORAGE ELEMENT

Honorable Commissioner of  
Patents and Trademarks  
Washington, D.C. 20231

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JUL 11 1991  
GROUP 230

Dear Sir:

EXPLANATION UNDER RULE 1.608(b)

In September of 1984, Krysalis Corporation was formed to develop integrated nonvolatile memories to compete with other semiconductor memory suppliers. At that time, the standard nonvolatile memory in the industry relied on the tunneling effect of electrons through a thin layer to provide a residual charge, or the absence thereof, on the gate of a transistor to allow nonvolatile storage of data. Krysalis embarked on a development program to design a nonvolatile memory using ferroelectric material as the nonvolatile storage element. It is believed that no one

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(Date of Deposit)

Roger N. Chauza, Reg. No. 29,753

Name of applicant, assignee, or  
Registered Representative

*Roger N. Chauza*  
Signature

July 8, 1991  
Date of Signature

had actually developed an integrated ferroelectric memory before, and thus Krysalis had to develop: a ferroelectric material that was compatible with semiconductor processing techniques, the techniques and various materials by which the ferroelectric material could be deposited on a silicon wafer without deleterious effects to any of the material, and the actual integration of ferroelectric capacitors with silicon CMOS circuits on a semiconductor wafer.

The major problems to overcome by Krysalis Corporation in developing nonvolatile ferroelectric memories were thus twofold. First, a ferroelectric thin film material had to be developed which could be utilized in semiconductor memory applications. While ferroelectric ceramic material and its characteristics have been well known in the art for many years, the use thereof in microelectronic memory applications posed new problems. For example, it is well known that the traditional use of memories involved the repeated reading and writing of data therein. It is also well known that ferroelectric material exhibits a fatigue and aging characteristic, in that the repeated polarizing, and repolarizing of the domains in the ferroelectric material leads to a reduced life of the material. Such a characteristic is contradictory to its use in a memory application, which necessarily requires the repeated repolarization of the ferroelectric material during read and write operations.

Secondly, the integration of ferroelectric material with semiconductor devices, in a memory array, was an area not successfully encountered before. In other words, the processes for integrating ferroelectric thin film material and semiconductor devices had to be developed and verified to determine if indeed semiconductor nonvolatile memory arrays could be fabricated with ferroelectric thin film material. Contrary to the teachings of a significant

portion of the prior art, an adverse reaction occurs between semiconductor material and ferroelectric material, which adverse effects had to be identified and overcome.

Summary of the Evidence

Evidence submitted herewith establishes that silicon test wafers, termed "TD01" wafers, were designed and fabricated by Krysalis Corporation in late 1986. These wafers had a 2x2 array of ferroelectric, nonvolatile memory cells, connectable either as an array of four, single-transistor, single-ferroelectric capacitor memory cells, or an array of a pair of complementary memory cells each having two transistors, two ferroelectric capacitors and a complementary bit line. Both types of memory circuits were fabricated on the TD01 test wafers.

(Womack, Exhibits A-F)

Further evidence submitted herewith in the nature of engineering notebook pages (Womack, Exhibit G, Figs. 3 and 4) of Richard H. Womack show the prior conception of a memory cell having an access transistor and a corresponding ferroelectric capacitor for storing a data state. Particularly, Fig. 3 of Womack's engineering notebook shows an array of two single-transistor, single-capacitor memory cells that are individually accessible by different word lines, but have a common drive line and a common bit line. Mr. Womack's declaratory statements and supporting exhibits confirm that the nonvolatile memory cell specified in the proposed count was conceived well before the Eaton, Jr. '664 patent filing date.

The notebook pages bearing the relevant drawings and operational description of such a memory cell were entered by Mr. Womack in September and October, 1986, well before the February, 1987, filing date of the Eaton, Jr. 4,873,664 patent.

Because of limited Krysalis resources in terms of money and personnel, Krysalis pursued development of the complementary type of ferroelectric memory cell, rather than the single-transistor, single-capacitor memory cell. (Womack, Declaration ¶ 14). The complementary memory cell design was implemented by Mr. Womack into an "ECD512" memory device.

Mr. Womack designed and developed the "ECD512" nonvolatile memory chip having an array of 64x8 complementary memory cells, and with each complementary bit line connected to a sense amplifier. (Womack, Exhibits H-N) During the development of the "ECD512" memory, the parent of the above-captioned continuation patent application was prepared and filed in the U. S. Patent and Trademark Office.

Enclosed herewith also is a Declaration by Mr. Leo N. Chapin, together with attached exhibits, which verify the significant efforts and diligence by Krysalis in 1986 and 1987 in developing a ferroelectric material suitable for integration with silicon circuits on a semiconductor wafer. Mr. Chapin maintained a log of the many semiconductor and other types of wafers used in the development of a suitable ferroelectric material. Because of the substantial difficulties and problems involved in developing a ferroelectric material which had suitable ferroelectric characteristics and which was compatible with semiconductor wafers, numerous wafers and CMOS circuits were involved for evaluation purposes. The ferroelectric film processing log of Exhibit A of Mr. Chapin's Declaration illustrates that between August of 1986 and September of 1987, over 100 whole or partial wafers of various types and sizes were processed with numerous types of ferroelectric material and under

different processing conditions to achieve a composition suitable for use as a capacitor dielectric film on integrated CMOS wafers.

Enclosed also is a Declaration and exhibits by William D. Miller, a former President of Krysalis Corporation, evidencing the efforts of employees of Krysalis who developed and tested numerous compositions of ferroelectric thin film material for integration with memory circuits on semiconductor substrates. Mr. Miller's Declaration sets forth the time frame and the procurement of TD01 wafers (Miller, Exhibit 4) and 512 wafers (Miller, Exhibit 5) from a semiconductor foundry. The transistor circuits fabricated in the silicon wafers by the foundry were according to the circuit design of Mr. Womack, and thereafter Krysalis further processed the wafers to form the ferroelectric capacitors connected to the transistor circuits. In his Declaration, Mr. Miller confirms that a ferroelectric capacitor defines an essential component of Applicants' claimed nonvolatile memory. Indeed, the ferroelectric capacitor is the component of Applicants' memory cell which provides the mechanism for the nonvolatile storage of data states.

During the entire time period of 1987, which encompasses the critical time period, all the declarations and exhibits evidence that the Krysalis employees were diligent in conducting tests and further developing ferroelectric material for use with integrated memory circuits. Mr. Miller's Declaration further substantiates that the Krysalis efforts in developing ferroelectric material and nonvolatile memory circuits were carried out in the United States of America.

The Declarations of Leo N. Chapin and Joseph T. Evans, Jr., and the respective exhibits attached thereto, illustrate the substantial activity during the critical

time period in developing and characterizing the electrical properties of ferroelectric materials developed by Krysalis. Mr. Joseph T. Evans, Jr.'s declaration further shows that Krysalis submitted to its patent attorney an invention disclosure covering the ferroelectric memory cell architectures of both the single-transistor, single-capacitor cell and the complementary cell (2 cells per bit) for the preparation of a patent application. Krysalis personnel believed that both cell architectures were related to the same general invention. (Evans, Declaration ¶ 3).

Additional evidence of diligence submitted herewith is in the nature of a Declaration by an attorney representing Krysalis Corporation. The attorney, Mr. Nixon, prepared the patent application parent to the above-captioned continuation application. In November, 1986, Mr. Nixon discussed the details of both the single-transistor, single-ferroelectric capacitor memory cell and the complementary ferroelectric memory cell with Mr. Womack. (Nixon, Exhibit A) Between early March, 1987, and Applicants' June 2, 1987, patent filing date, the attorney prepared the parent of the above-captioned patent application and received revisions by the inventors. (Nixon, Exhibits B-O)

The Applicants' work conducted in reducing the complementary cell architecture memory to practice, while perhaps outside the scope of the count related to the single-transistor, single-capacitor architecture, can yet be used for purposes of diligence, when the inventions were considered to be related and filed in the same patent application. De Solms v. Schoenwald, 15 USPQ2d 1507 (Bd. Pat. Int. 1990).

An attorney's diligence in preparing a patent application is evidence that can be used in the consideration of diligence in reducing the invention to practice. Rines v. Morgan, 250 F.2d 365, 116 USPQ 145 (CCPA 1957).

The diligence of inventors in the actual reduction of the invention to practice can be coupled with the diligence of attorneys in the constructive reduction to practice by preparing a patent application on the invention. Gammeter v. Backdahl, 267 F. 347, 1920 C.D. 209 (App. D.C. 1920).

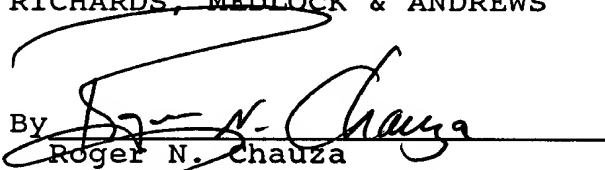
Conclusion

Based on the Declarations of the inventors and other persons, and the respective exhibits, it is submitted that there is ample evidence to establish a prima facie case of priority of the claimed invention before the filing date of the Eaton, Jr. patent. It is respectfully requested that an interference be declared between the captioned patent application and the Eaton, Jr. '664 patent.

Respectfully submitted,

RICHARDS, MEDLOCK & ANDREWS

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